



# **CMS GCT Hardware LANL Contributions**

2006 - 2007

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# Background



- Global calorimeter Trigger
  - Processes all trigger data from Hadronic and Electron calorimeters
  - Identifies jet objects
    - Electron objects identified upstream by regional Calorimeter Trigger
  - Sorts both electron and jet objects
    - Determines the 4 highest ranked objects
  - Forwards data to Global Trigger
    - Where Calorimeter and Muon data are combined



# History

- Originally assigned to Bristol University
  - Large 9U VMR based design
  - System design reasonable
  - Implementation inadequate
    - Power, grounding, and communication problems
    - Over budget and behind schedule
  - CERN stopped development and assumed responsibility 1/06
    - Appointed LANL TSM at CERN project engineer
      - Allowed freedom to contract for LANL resources and utilize CERN capabilities as appropriate



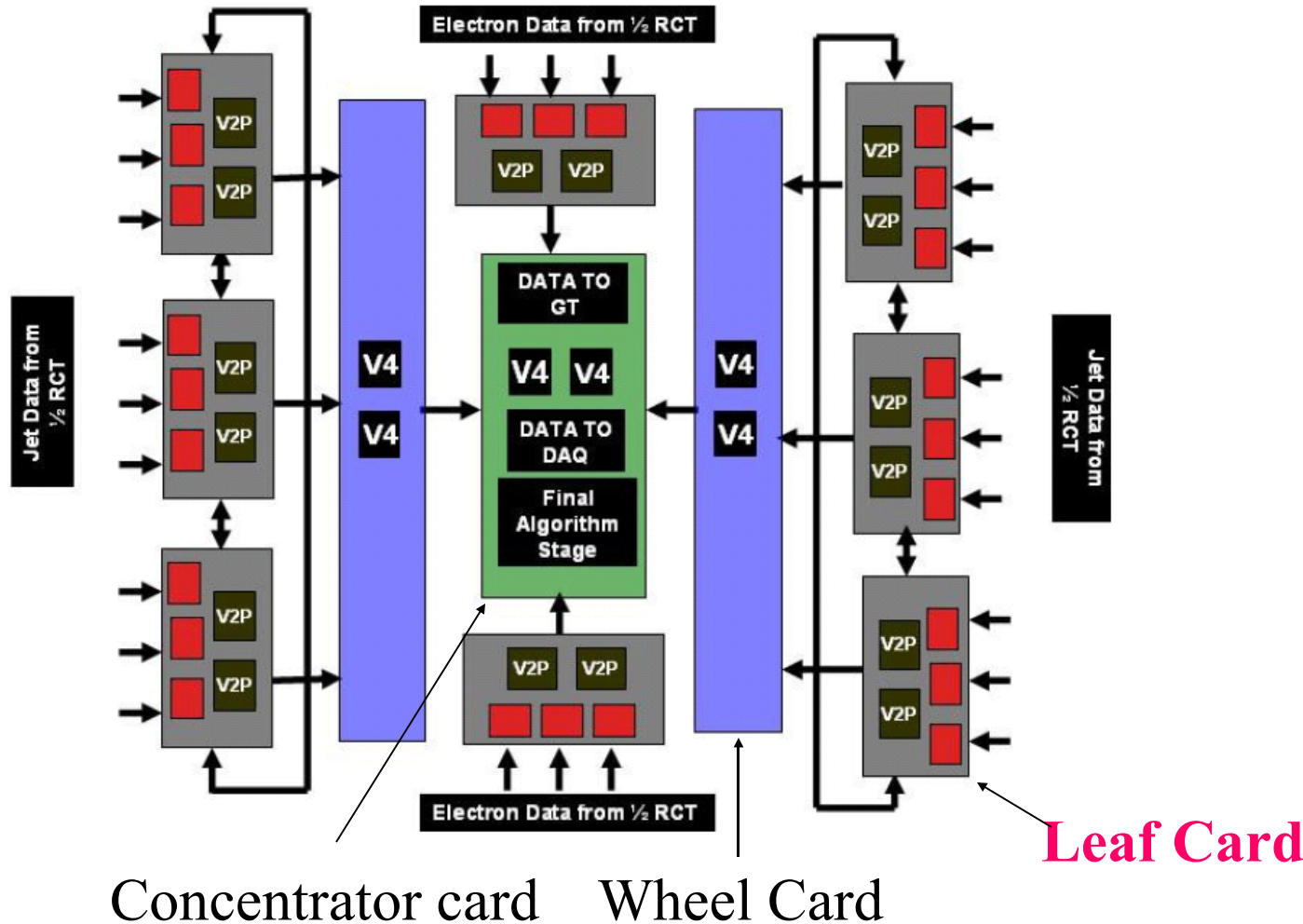
# GCT Design



- Three main elements
  - Leaf card, main processing element
  - Wheel card, half barrel object sorting
  - Concentrator card, global sorting and control
- LANL contributions
  - Leaf card design and production
  - Wheel card design (CERN production)
  - Overall system engineering responsibility



# GCT Block Diagram





# Leaf Card Functions



- Receive Data from RCT
  - Jet Data from 3 crates
  - Electron data from 9 crates
- Output partially processed data
  - Pre-clustered jets
    - From each crate
  - Electron trigger candidates
    - From each half-barrel
- Share data with adjacent Leaf
  - Required for jets spanning RCT crate boundary
- Input Format
  - Optical links operating at 1.6 Gbps
    - Two links correspond to one RCT output cable
- Output Format
  - Parallel data at 40MHz DDR single ended to wheel/concentrator card
  - Parallel data at 40MHZ DDR differential to adjacent leaf



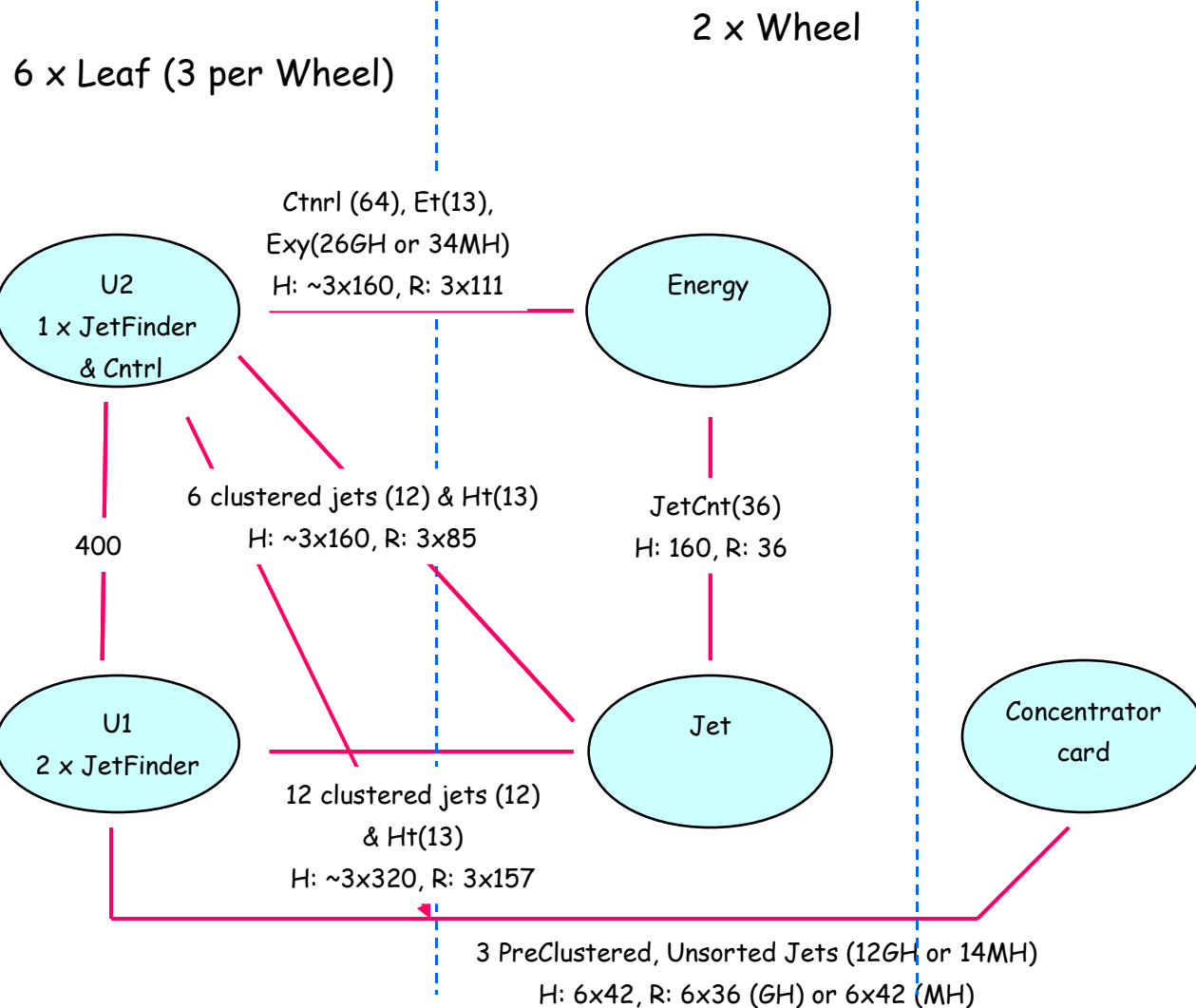
# Hardware Connectivity



- Accepts data on 3, 12 channel serial optical links
  - 32 receivers implemented
    - 2.5 Gb/sec, 1.6 Gb/sec required
  - Handles 3 RCT crates (jet), 9 RCT crates (electron)
- Shares data with neighbors
  - Jet only
  - 60 LVDS pairs to each neighbor
- Outputs parallel data
  - Jet data processed further on wheel card
    - Count
    - 4 highest Et
  - Electron data processed further on concentrator card
    - 4 highest Et
  - Electrical interface
    - 338 single ended signals provided



# Leaf bus output capacity

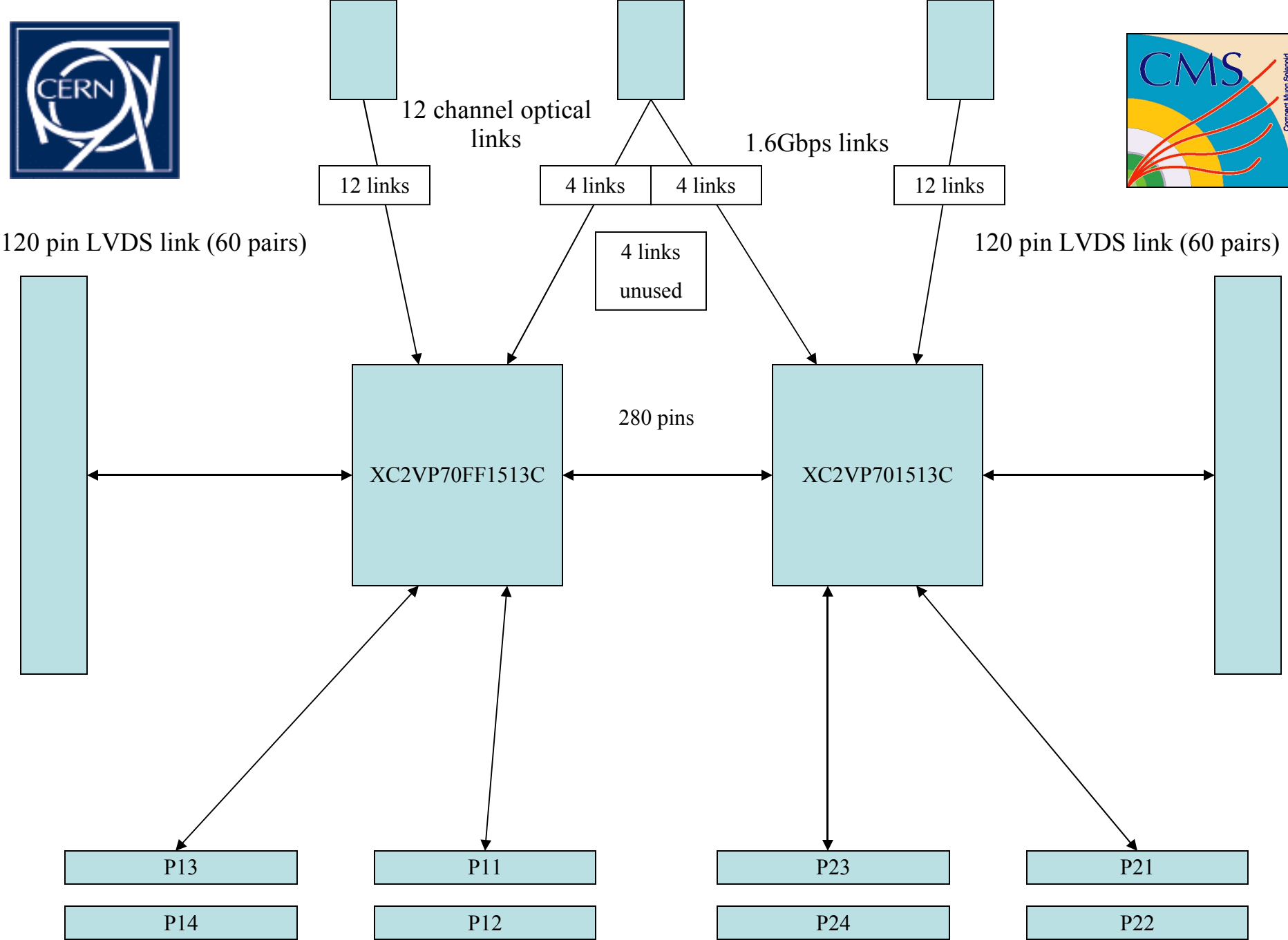




# Implementation



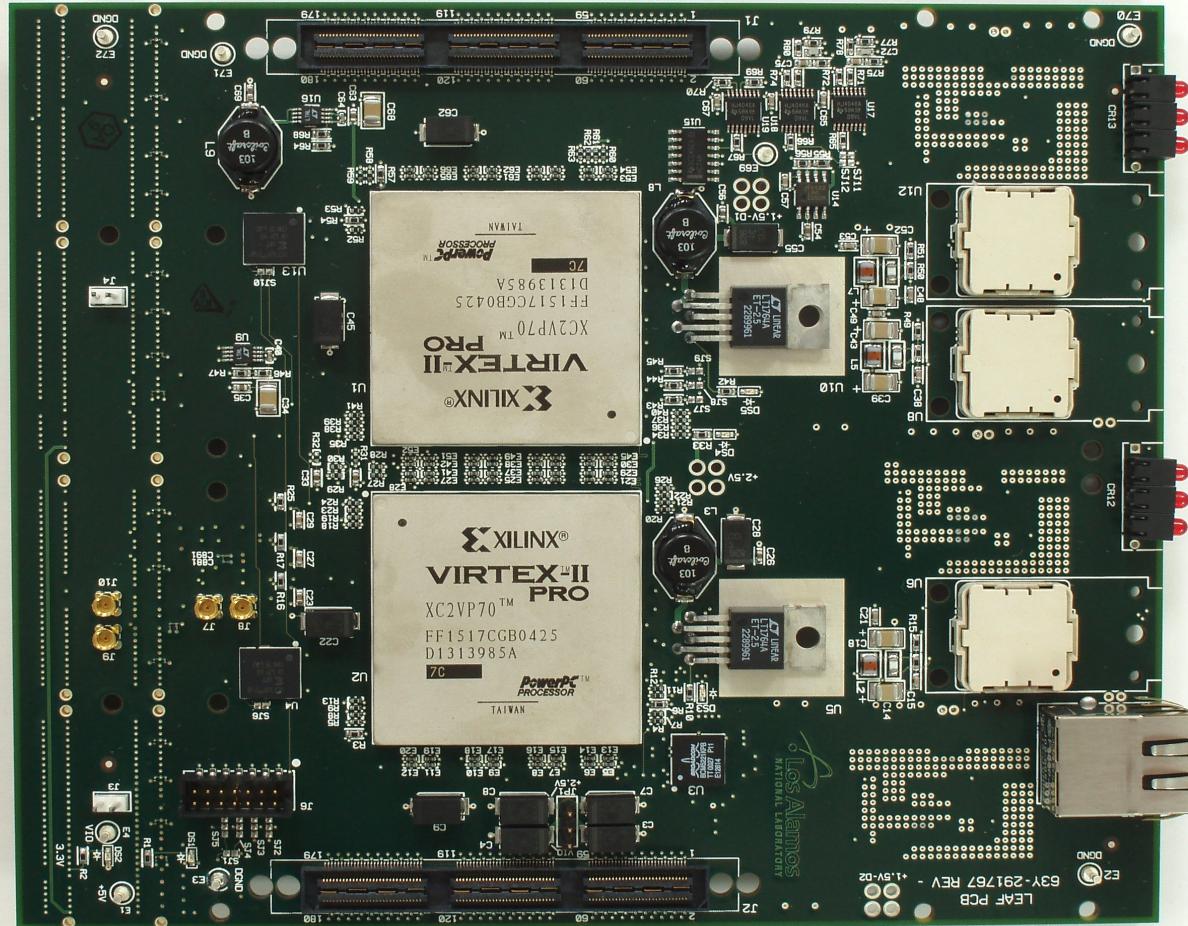
- High density Optical Inputs
  - Cannot fit enough SFP single channel modules
  - “Snap 12” parallel receiver
    - 12 channels at 2.5Gbps
      - Industry standard short distance link
- Xilinx Embedded SERDES links (Rocket I/O)
  - Virtex2 Pro devices selected
    - V2P50/70 with 16 links each
    - Support improved differential I/O
    - Easily obtainable
- No external (off FPGA chip) memory
  - Nice to have, but not required for GCT processing
- Double PMC format
  - Power supply and basic layout retained from existing design
  - Electrically compatible, but too high mechanically
    - Not truly PMC compliant

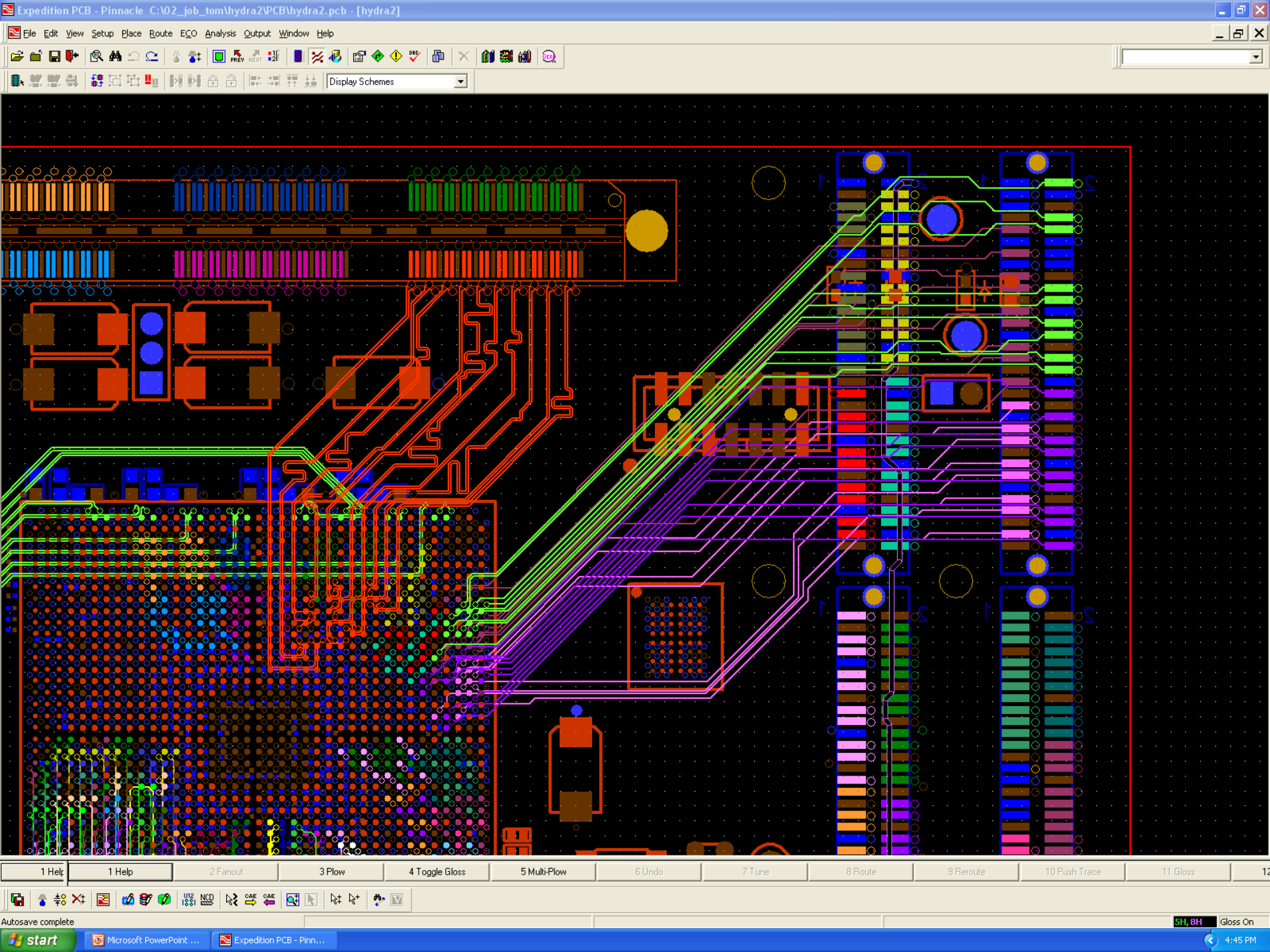


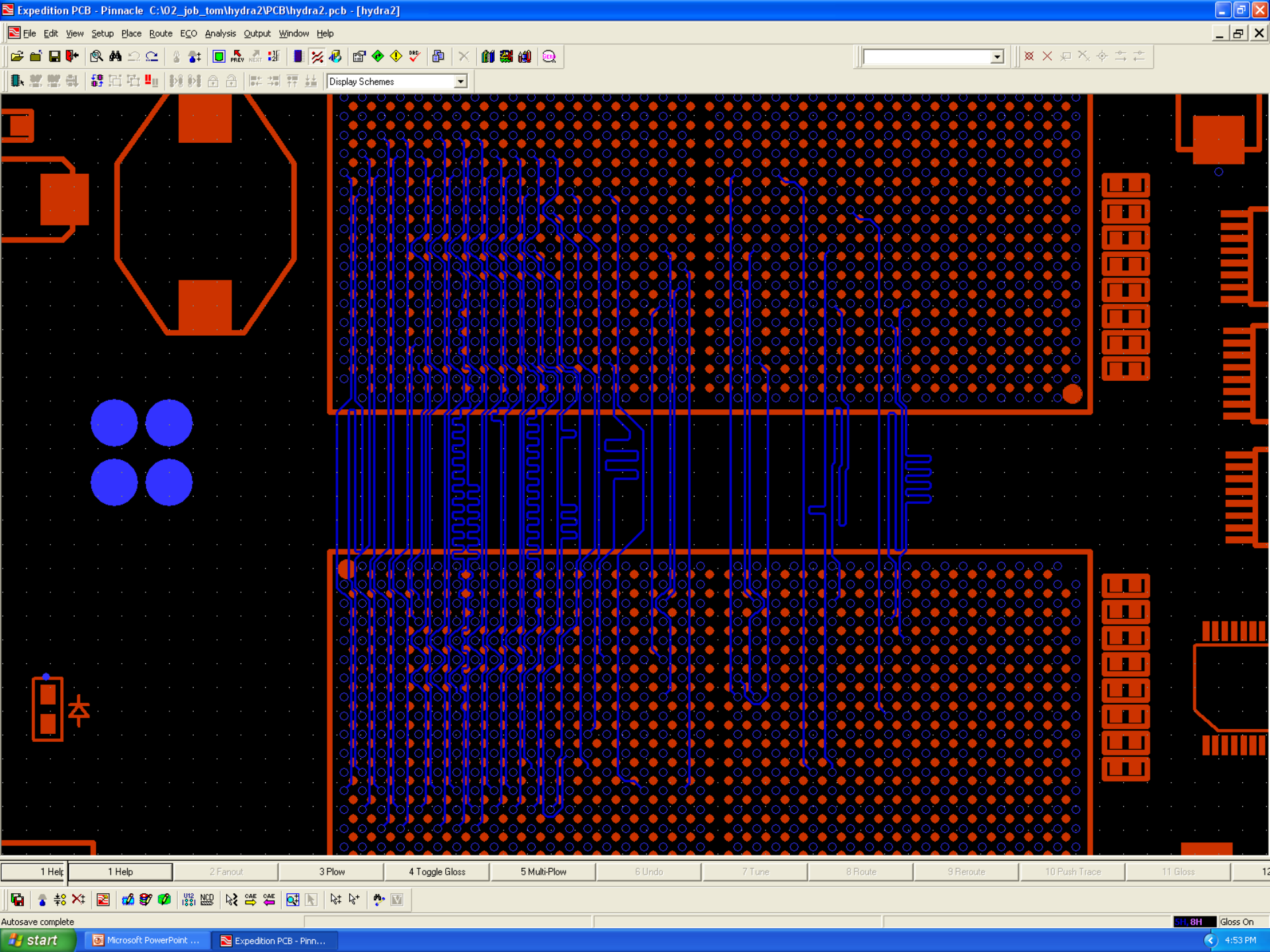
Fully populated PMC I/O – 338 usable pins



# Leaf









# Electrical Interfaces



- LVDS signalling
  - V2Pro supports true 100 Ohm termination
    - ~240mA for 60 pairs
  - Samtec QTS/H differential connectors
    - High density and speed
      - Rated for multi GHz operation
    - Commercial cable assemblies
- DDR used for all single ended I/O
  - FPGA intercommunication at 40MHz
    - Use DCI (50 Ohm) or 6mA current limit
      - Less than 2A assuming 200 interconnects
  - Communication with Wheel card at 40MHz
    - Use DCI (50 Ohm) or 8-12mA current limit
      - 4.5A assuming 368, 12mA interconnects
        - » Will be less
    - Board supports adhesive heat sinks
      - 5V fan headers if required



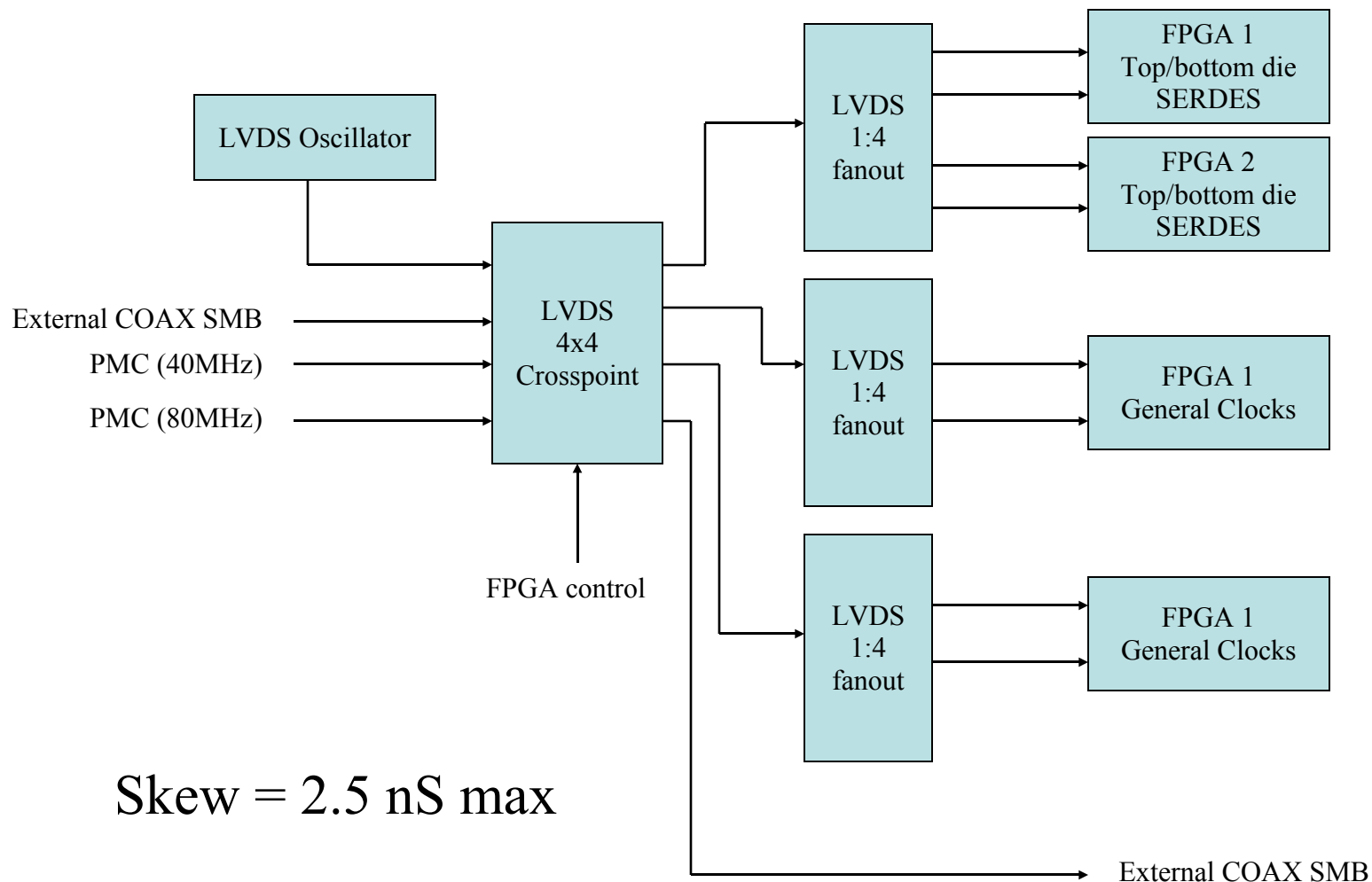
# Routing Parameters



- Length matching
  - Differential lines matched to  $\frac{1}{4}$ " as a bus
    - Yields  $\frac{1}{2}$ " on board/board connections
      - Individual pairs matched to a few mils
    - Matched in groups of 8 pairs
    - Not required for 40MHz DDR
      - Allows significant speed increase
  - Single ended lines matched to  $\frac{1}{2}$ " as a bus
    - Matched in groups of 8-12 lines
    - Not required for 40MHz DDR
      - Allows higher speed operation
  - Differential SERDES lines matched to 1-2 mils
    - Impedance controlled and individually matched
- Plane structure not finalized yet
  - Based on existing design, but will need to be modified



# Clock Tree



single ended clocks (2 per FPGA) tie directly to PMC



# Power supplies



- 15A, 1.5V switcher for each V2Pro VccInt
  - Devices can be run at thermal limit
    - Fan headers on board if needed
    - Estimated load less than 1/2 this figure
      - 40MHz, 100% utilization yields 6A
- Single 15A, 2.5V switcher for I/O
  - Estimated load is 1/2 of this capacity
- Switchers powered from 5V
  - Not used for other logic
  - Phase and frequency controlled
    - Can optimize noise or efficiency
    - Switch out of phase to control surge currents
- Separate linear supplies for SERDES
  - Each FPGA has local linear SERDES supply
- Optical receivers powered directly from 3.3V PMC power
  - Manufacturer claims this is acceptable



# Wheel Card Functions



- Carries 3 leaf cards (double PMC)
  - Compresses (sorts) Jet data
  - Calculates Et and Jet count
  - Single ended electrical interface (DDR 40MHz)
- Extra PMC planned
  - Muon bits
  - Not used for initial functionality
- Interfaces to concentrator board
  - High speed cable interface
  - LVDS electrical interface
    - Virtex4 – Virtex4 links
    - DDR 40Mhz required, but could support much higher
- 9U VME form factor
  - Power only, no VME interface
    - ECAL backplane



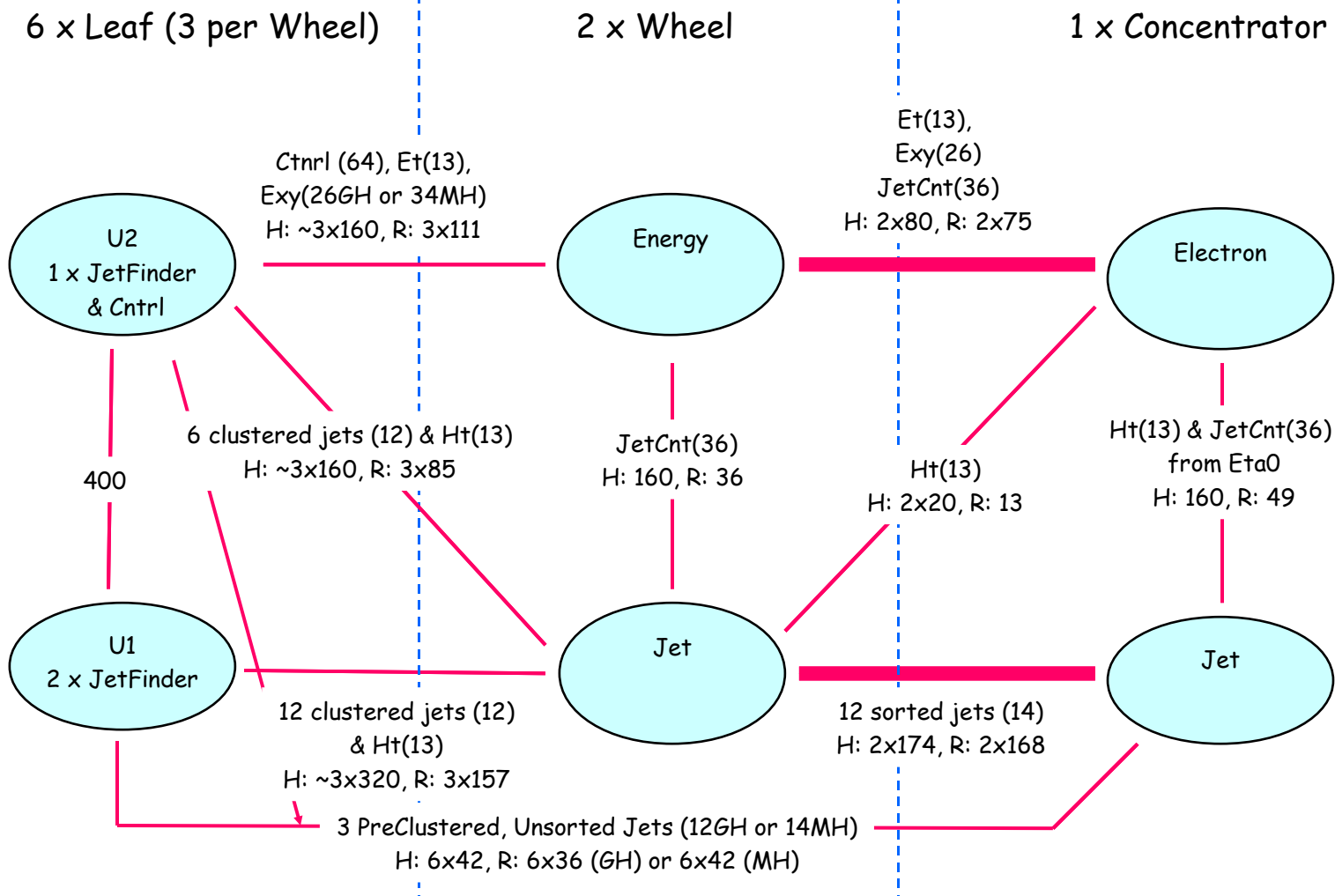
# Hardware Connectivity



- Accepts parallel data from leafs on 3 DPMC sites
  - 338 signals on each site (total 1014)
    - Single ended
- Extra PMC site for future use
  - 169 signals
- Outputs parallel data
  - Jet data processed further on concentrator card
    - Count
    - 4 highest Et
  - Electrical interface
    - 240 differential pairs provided



# Wheel data bus capacity





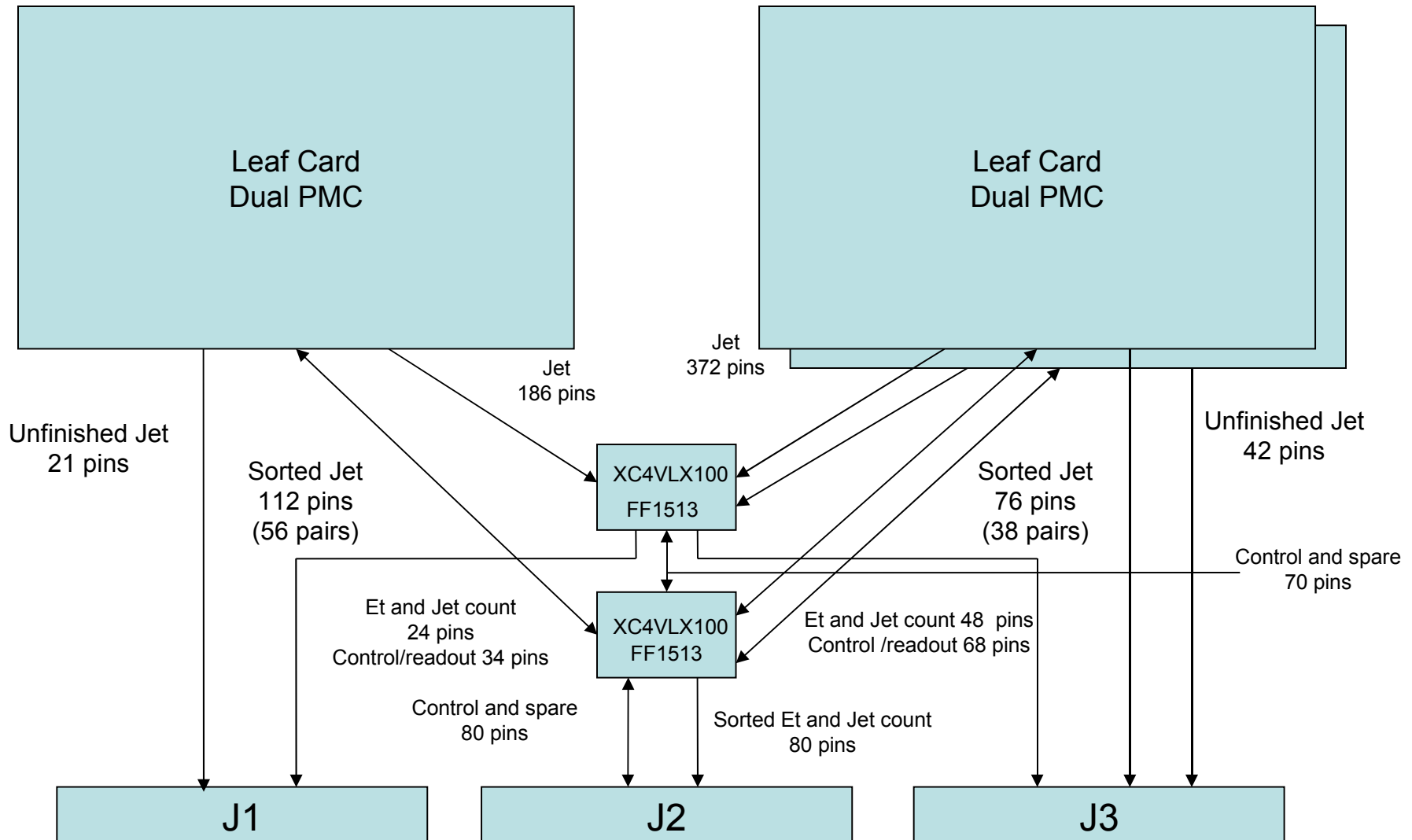
# Implementation



- Data handling
  - Accepts data from 3 leaf cards
    - Not enough I/O to pass all information through FPGAs
  - Passes through unfinished Jet data
    - 63 signals bypass
      - Through dedicated differential drivers
  - FPGAs drive remaining signals directly
- Processing
  - Two Xilinx Virtex4 FPGAs
  - XC4VLX100FF1513
    - I/O (as opposed to logic) intensive design
    - Advanced Virtex4 I/O features reduce risk
      - Better double/quad data rate support
      - Improved Differential support
  - One for Jet sorting, one for Et and Jet count

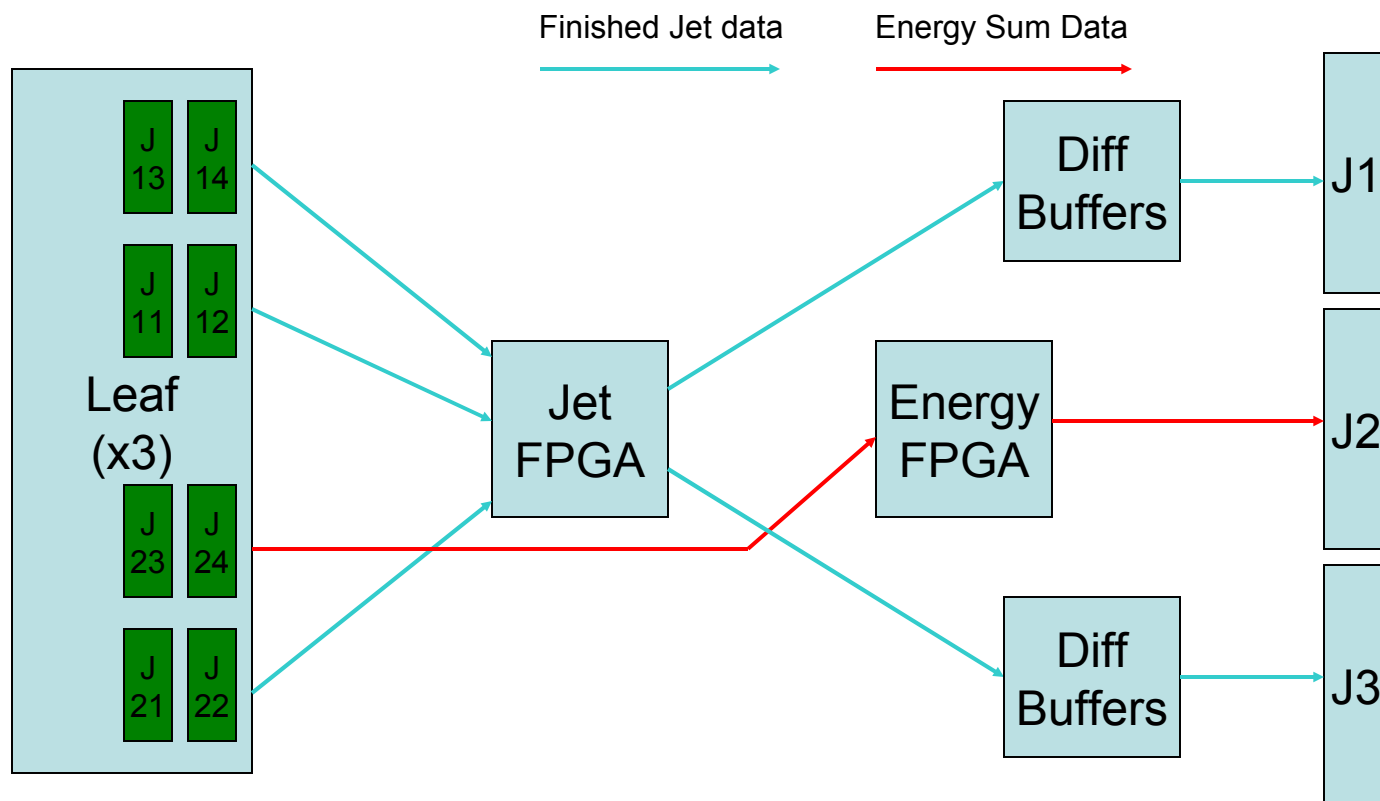


# Block Diagram





# Wheel Card – Data Flow





# Electrical Interfaces



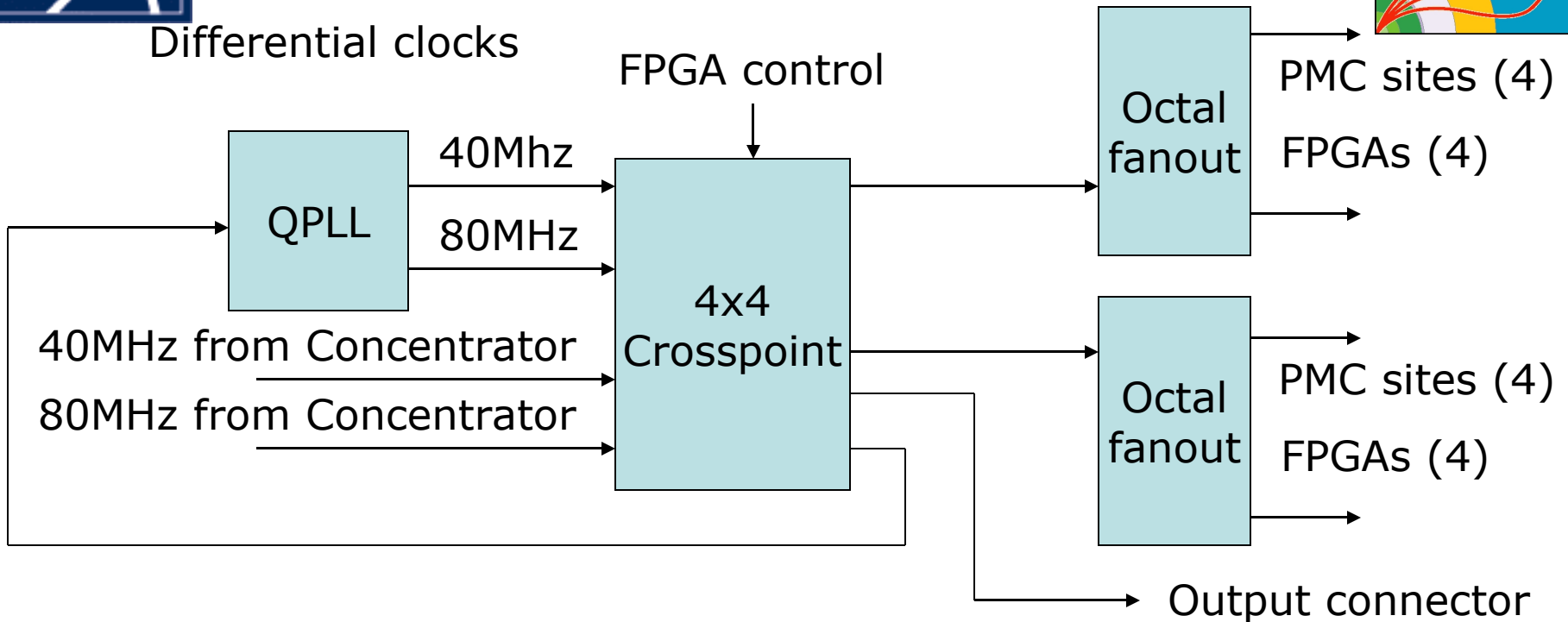
- LVDS signaling
  - V4 drives directly
    - 40MHz DDR required, but can support much faster
      - V4 receivers on concentrator allow maximum flexibility
  - Samtec QTS/H differential connectors
    - High density and speed
      - Rated for multi GHz operation
    - Commercial cable assemblies
- DDR used for all single ended I/O
  - FPGA intercommunication at 40MHz
    - Short runs allow faster operation
  - Communication with Leaf cards at 40MHz
    - PMC connectors limit speed here
      - 338 signals provide margin for growth
- Direct connection of 21 signals per Leaf to Concentrator
  - Dedicated LVDS drivers
    - Not clocked
  - Intended for unfinished jet ( $\eta = 0$ ) data



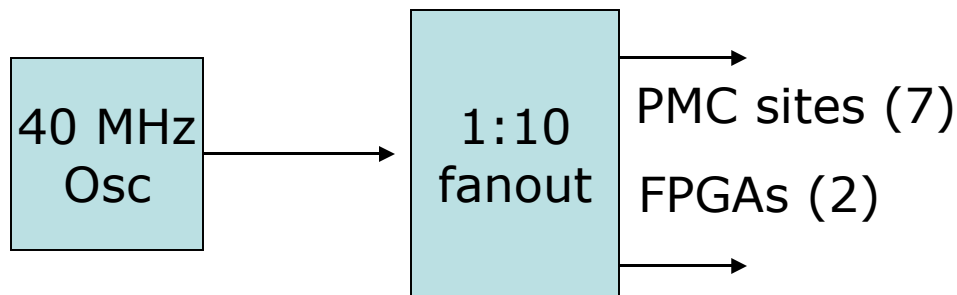
# Clock Tree



Differential clocks



Single ended clocks





# Power supplies



- 10A, 1.2V switcher for each V4 VccInt
  - Devices can be run near thermal limit
    - Fan headers on board if needed
    - Estimated load less than 1/2 this figure at 40MHz
- Two 10A, 2.5V switchers for I/O
  - Leaf cards may be jumpered to provide own VIO
    - Wheel will only need to drive own FPGAs
- 10A, 3.3V switcher for each DPMC site
  - Board design allows for substitution of 5A Linear
    - Would be preferable since optical receivers are powered directly
    - Questionable margin requires switcher site be provided
- All Switchers powered from 5V
  - Not used for other logic
- Separate linear supply for QPLL and some clock distribution
  - 2.5V



# FPGA loading and control



- JTAG
  - CPLD JTAG switch controls 7 independent chains
    - Single JTAG header switched to multiple chains
    - Individual chains can be daisy chained together or bypassed
    - JTAG interface vial front paned connector or concentrator
    - Configured by front panel switches
    - 3.3V external interface
    - CPLD reprogrammable by dedicated JTAG connector only
  - Individual JTAG chains
    - 4 devices, 2 FPGAs and 2 FLASH PROMs
- Default FPGA configuration via Xilinx FLASH PROM
  - Single platform FLASH XCF32P per device
- Control via concentrator card
  - USB test fixture for stand alone operation
- No dedicated global reset
  - Define logic reset lines in firmware
  - Utilize JTAG for device reprogramming